

CHARACTERIZING THE $I_{gs}(V_{gs})$ NONLINEARITY FOR DESCRIBING ITS CONTRIBUTION TO FET LARGE-SIGNAL INTERMODULATION DISTORTION

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ABSTRACT

In this paper, a simple procedure for extracting the $I_{gs}(V_{gs})$ Taylor-series coefficients along a load line is presented, as a way to accurately characterize its contribution to FET large-signal intermodulation distortion (IMD) behaviour.

INTRODUCTION

Modern wireless systems should handle a bandpass modulated signal with a strongly varying envelope. The need for providing high linearity without losing efficiency, has determined a tremendous interest on power amplifier linearization at both academic and industrial communities. Device-level linearization techniques are here standing as real alternatives to system level approaches, mainly when a low cost and compact solution is required.

The control over the large-signal intermodulation distortion, and particularly the use of the linearity sweet-spots, has been possible thanks to recent advances on the understanding of the device behaviour [1]. Most of the published work has been focussed on the role of the main nonlinearity, the $I_{ds}(V_{gs})$ characteristic along the power amplifier load line. However, a few attempts have been made to determine the influence of the secondary nonlinearities [2].

In this paper, an experimental procedure for the simultaneous extraction of the $I_{gs}(V_{gs})$ and the $I_{ds}(V_{gs})$ Taylor-series coefficients is presented. Based on previous techniques [3], [4], the corresponding input and transfer derivatives are obtained from harmonic distortion measurements on gate and drain side.

DERIVATIVE EXTRACTION TECHNIQUE

In Fig. 1, the test set-up for input and output harmonic distortion measurement is presented. Special care was put on avoiding undesired contributions from the device reactive nonlinearities as well as undesired distortion coming from the signal generator, the amplifier, and the spectrum analyzer.

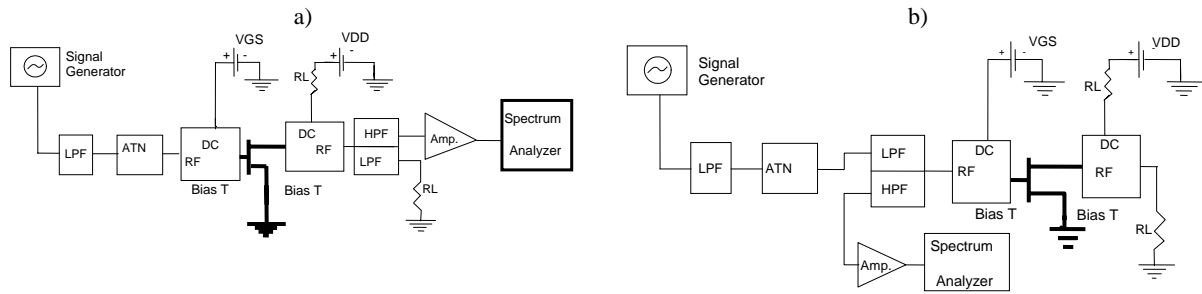


Fig. 1 Test set-up for harmonic distortion measurement on a) drain and b) gate side.

Using the nonlinear current technique for Volterra-series analysis, the second and third order $I_{gs}(V_{gs})$ and $I_{ds}(V_{gs})$ derivatives, Ggs_2 and Ggs_3 as well as Gm_2 and Gm_3 can be respectively obtained,

$$Ggs_2 = \frac{2 \cdot [1 + Gm_1 \cdot R_s + Ggs_1 \cdot (R_{gen} + R_g + R_s)]^2}{V_{gen}^2(\omega)}$$

$$[I_{gs}(2\omega) \cdot (1 + Ggs_1 \cdot (R_{gen} + R_g + R_s)) + I_{ds}(2\omega) \cdot Ggs_1 \cdot R_s] \quad (1)$$

$$Gm_2 = \frac{2 \cdot [1 + Gm_1 \cdot R_s + Ggs_1 \cdot (R_{gen} + R_g + R_s)]^2}{V_{gen}^2(\omega)}$$

$$[I_{ds}(2\omega) \cdot (1 + Gm_1 \cdot R_s) + I_{gs}(2\omega) \cdot Gm_1 \cdot (R_{gen} + R_g + R_s)] \quad (3)$$

$$Ggs_3 = \frac{4 \cdot \left[1 + Gm_1 \cdot R_s + Ggs_1 \cdot (R_{gen} + R_g + R_s) \right]^3}{Vgen^3(\omega)} \quad (2)$$

$$\left[Igs(3\omega) \cdot (1 + Ggs_1 \cdot (R_{gen} + R_g + R_s)) + Ids(3\omega) \cdot Ggs_1 \cdot R_s \right] + \frac{2Ggs_2 \cdot [Ggs_2 \cdot (R_{gen} + R_g + R_s) + Gm_2 \cdot R_s]}{[1 + Gm_1 \cdot R_s + Ggs_1 \cdot (R_{gen} + R_g + R_s)]}$$

$$Gm_3 = \frac{4 \cdot \left[1 + Gm_1 \cdot R_s + Ggs_1 \cdot (R_{gen} + R_g + R_s) \right]^3}{Vgen^3(\omega)} \quad (4)$$

$$\left[Ids(3\omega) \cdot (1 + Gm_1 R_s) + Igs(3\omega) \cdot Gm_1 \cdot (R_{gen} + R_g + R_s) \right] + \frac{2 \cdot Gm_2 \cdot [Ggs_2 \cdot (R_{gen} + R_g + R_s) + Gm_2 \cdot R_s]}{[1 + Gm_1 + Ggs_1 \cdot (R_{gen} + R_g + R_s)]}$$

A typical PHEMT device, a NE3210s01 from NEC semiconductors, was then characterized. In Fig. 2, the extracted derivatives are shown in terms of the extrinsic voltage.

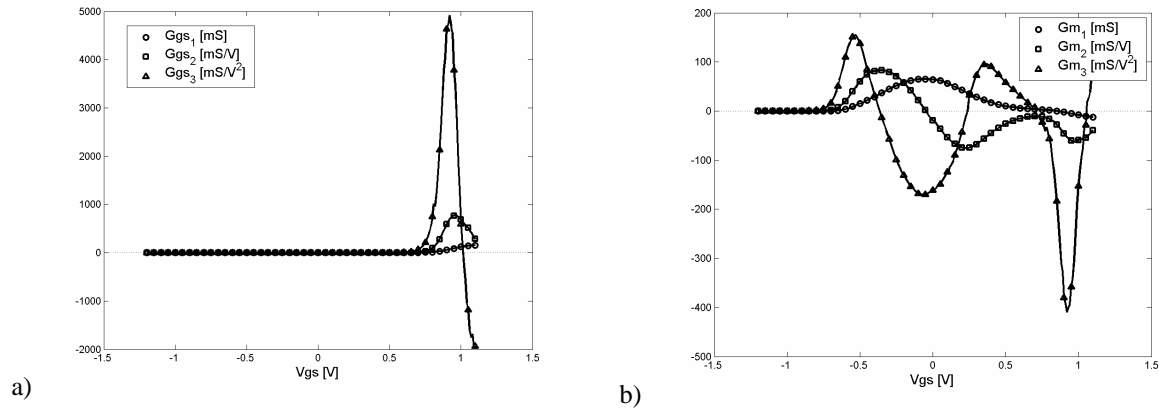


Fig. 2 Evolution with V_{GS} for $V_{DD}=3V$ and over a 50Ω load line: a) $I_{gs}(V_{gs})$ derivatives and b) $I_{ds}(V_{gs})$ derivatives.

As it can be observed, the $I_{gs}(V_{gs})$ derivatives correspond to the expected behaviour from an exponential nonlinearity in series with a linear resistor. G_{gs1} tends to a saturation value, $1/R_i$, and the null of G_{gs3} would allow an accurate definition of the diode knee voltage. G_{m1} may take a negative sign for high V_{GS} values, due to the diode presence and the role of the feedback R_s resistor.

In the conduction range of the gate-to-source diode, the input nonlinearity really affects the transfer one. For high load values, this range is far apart from the region of transconductance compression, reason why no significant influence over the large-signal sweet-spot could be expected. When interested in getting the highest signal excursion for output power maximization, the situation is however different. The transconductance compression nearly coincides with the input diode conduction. In such condition, it seems that the input resistive nonlinearity could influence the sweet-spot position if adequate values were used for the gate impedance conditions. Simulation results seem to support this small role. Adding a gate bias resistor, it has been also proved that the sweet-spot position could be adjusted to the input power level [5].

CONCLUSION

A simple procedure for extracting the $I_{gs}(V_{gs})$ Taylor-series coefficients along a load line has been presented, as a way to accurately characterize this nonlinearity contribution to FET large-signal intermodulation distortion (IMD) behaviour. The possibility of using its contribution for linearity improvement, with the aid of the out of band gate impedance values, would have to be explored.

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